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## 1 [Instruction set extensions for software defined radio on a multithread](#)

 [Suman Mamidi, Emily R. Blem, Michael J. Schulte, John Glossner, Daniel Iancu, Mayan Moudgill, Sanjay Jinturkar](#)

 September 2005 **CASES '05**: Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems

**Publisher:** ACM

 Full text available:  Pdf (189.05 KB) Additional Information: [full citation](#), [abstract](#), [references](#)
**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 57, Citation (6 Weeks): 1, Citation (12 Months): 1

Software defined radios, which provide a programmable solution for improving physical layer processing of multiple communication standards, are widely considered one of the most important new technologies for wireless communication.

**Keywords:** Reed-Solomon coding, Viterbi decoding, convolutional encoder, signal processor, forward error correction, instruction set extensions, multithreaded software defined radio, turbo decoding

## 2 [Low-power asynchronous viterbi decoder for wireless applications](#)

 [Mohamed Kawokgy, C. André T. Salama](#)

 August 2004 **ISLPED '04**: Proceedings of the 2004 international symposium on Low-power electronics and design

**Publisher:** ACM

 Full text available:  Pdf (220.30 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [terms](#)
**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 21, Citation (6 Weeks): 0, Citation (12 Months): 0

This paper describes the implementation of an asynchronous 64-state, pipelined Viterbi decoder using an original architecture and design methodology. The decoder is suitable for wireless communications applications, where bit rates over 100 Mb/s are required at a minimum ...

**Keywords:** VHDL, asynchronous, bundled-data, digital signal processing, handshaking protocol, low-power, register transfer level, speed-independent, synchronous, viterbi algorithm, wireless

## 3 [Low power architecture of the soft-output Viterbi algorithm](#)

 [David Garrett, Mircea Stan](#)

 August 1998 **ISLPED '98**: Proceedings of the 1998 international symposium on Low-power electronics and design


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**Publisher:** ACM


Full text available:  Pdf (758.59 KB) Additional Information: [full citation](#), [abstract](#), [reference terms](#)

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An important technique for reducing power consumption in VLSI system reduction, the substitution of a less-costly operation such as a shift, for operation such a multiplication. Using a logarithmic number representa


**Keywords:** SOVA, VA, low power, turbo codes

#### 4 [Reconfigurable platforms for ubiquitous computing](#)

 [Manfred Glesner](#), [Thomas Hollstein](#), [Leandro Soares Indrusiak](#), [Peter Zipl](#), [Mihail Petrov](#), [Heiko Zimmer](#), [Tudor Murgan](#)

April 2004 **CF '04**: Proceedings of the 1st conference on Computing frontier

**Publisher:** ACM


Full text available:  Pdf (479.97 KB) Additional Information: [full citation](#), [abstract](#), [reference terms](#)

**Bibliometrics:** Downloads (6 Weeks): 6, Downloads (12 Months): 100, Citation

Ubiquitous computing requires flexibility. Meeting distributed electronic everyday's life implies the need to adapt to evolving standards and dynamic environments. Furthermore, to gain user acceptance, such devices should adapt ...

**Keywords:** communication, dynamic power management, networks-on-reconfigurable hardware, reconfigurable processors, reconfiguration, ubiquitous computing

#### 5 [A low power Viterbi decoder implementation using scarce state transition pruning scheme for high throughput wireless applications](#)

 [Jie Jin](#), [Chi-Ying Tsui](#)

October 2006 **ISLPED '06**: Proceedings of the 2006 international symposium on electronics and design

**Publisher:** ACM


Full text available:  Pdf (332.13 KB) Additional Information: [full citation](#), [abstract](#), [reference terms](#)

**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 69, Citation (

This paper presents a low power Viterbi decoder design based on Scarce Transition (SST). We propose an approach which seamlessly integrates techniques with the SST decoding to reduce the average add-compare-computation. ...


**Keywords:** Viterbi algorithm, convolutional code, low power

#### 6 [MetaCores: design and optimization techniques](#)

 [Seapahn Meguerdichian](#), [Farinaz Koushanfar](#), [Advait Morge](#), [Dusan Petran](#), [Potkonjak](#)

June 2001 **DAC '01**: Proceedings of the 38th conference on Design automation

**Publisher:** ACM

Full text available:  [Pdf](#) (283.78 KB) Additional Information: [full citation](#), [abstract](#), [referen](#)  
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**Bibliometrics:** Downloads (6 Weeks): 10, Downloads (12 Months): 42, Citation

Currently, hardware intellectual property (IP) is delivered at three levels: hard, firm, and soft. In order to further enhance performance, efficiency of IP design, we have developed a new approach for designing hardware

**7** [Design of low-power high-speed maximum a priori decoder architecture](#)  
[A. Worm](#), [H. Lamm](#), [N. Wehn](#)


March 2001 **DATE '01**: Proceedings of the conference on Design, automatic Europe

**Publisher:** IEEE Press

Full text available:  [Pdf](#) (129.21 KB) Additional Information: [full citation](#), [references](#), [cited](#)


**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 9, Citation C

**8** [Vectorizing for a SIMdD DSP architecture](#)

 [Dorit Naishlos](#), [Marina Biberstein](#), [Shay Ben-David](#), [Ayai Zaks](#)

October 2003 **CASES '03**: Proceedings of the 2003 international conference architecture and synthesis for embedded systems

**Publisher:** ACM


Full text available:  [Pdf](#) (301.45 KB) Additional Information: [full citation](#), [abstract](#), [referen](#)  
[terms](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 60, Citation (

The Single Instruction Multiple Data (SIMD) model for finegrained parallelism recently extended to support SIMD operations on disjoint vector elements. In this paper we demonstrate how SIMdD (SIMD on disjoint data) supports effective

**Keywords:** SIMD, compiler controlled cache, data reuse, rotating register, parallelism, vectorization, viterbi

**9** [VLSI implementation of SISO arithmetic decoders for joint source ch](#)

 [Simone Zezza](#), [Guido Masera](#)

March 2008 **DATE '08**: Proceedings of the conference on Design, automatic Europe


**Publisher:** ACM

Full text available:  [Pdf](#) (129.33 KB) Additional Information: [full citation](#), [abstract](#), [referen](#)

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 10, Citation (

In this paper we propose an efficient VLSI implementation of a Soft Input Soft Output (SISO) arithmetic code (AC) decoder for joint source channel coding. The application shows a very high level of processing complexity, but, to the

**10** [A dynamically reconfigurable adaptive viterbi decoder](#)

 [Sriram Swaminathan](#), [Russell Tessier](#), [Dennis Goeckel](#), [Wayne Burleson](#)

February 2002 **FPGA '02**: Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays

**Publisher:** ACM


Full text available:  [Pdf](#) (235.26 KB) Additional Information: [full citation](#), [abstract](#), [referen](#)

**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 70, Citation (

The use of error-correcting codes has proven to be an effective way to combat corruption in digital communication channels. Although widely-used, the communications decoding algorithm, the Viterbi algorithm, requires an

**Keywords:** FPGA, Viterbi coding, dynamic reconfiguration

**11** [A reconfigurable application specific instruction set processor for convolutional turbo decoding in a SDR environment](#)

 [Timo Vogt, Norbert Wehn](#)

March 2008 **DATE '08:** Proceedings of the conference on Design, automatic Europe

**Publisher:** ACM

Full text available:  Pdf (527.34 KB) Additional Information: [full citation](#), [abstract](#), [reference](#)

**Bibliometrics:** Downloads (6 Weeks): 11, Downloads (12 Months): 60, Citation (


Future mobile and wireless communication networks require flexible mobile architectures to support seamless services between different network standards on a common hardware platform that can support multiple protocols implemented and controlled by ...

**12** [BER evaluation and rate matching attribute selection for QoS support in WCDMA downlink](#)

[Joy Kuri, R. M. Karthik](#)

December 2008 **Wireless Networks**, Volume 14 Issue 6

**Publisher:** Kluwer Academic Publishers

Full text available:  Pdf (429.61 KB) Additional Information: [full citation](#), [abstract](#), [reference](#)

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 35, Citation (

In UMTS technology, Coded Composite Transport Channels (CCTrCh-s) consist of multiple Transport Channels (TrCh-s) in parallel on (usually) one physical connection. Rate Matching Attributes (RMA-s) are used to share the CCTrCh among ...

**Keywords:** UMTS, bit/frame error rate, mobile communication systems, rate matching attributes, wireless communication

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